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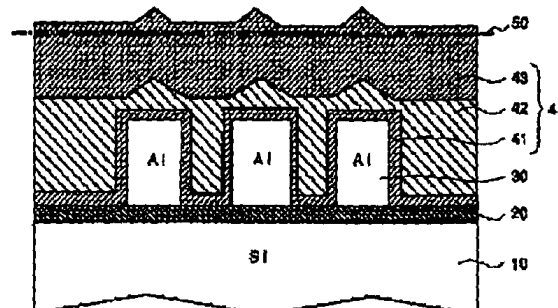
APPLICATION DATE : 22-09-97
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APPLICANT : HITACHI LTD;

INVENTOR : OKADA NOBUSUKE;

INT.CL. : H01L 21/768 H01L 21/316

TITLE : SEMICONDUCTOR INTEGRATED
CIRCUIT AND MANUFACTURE
THEREFOR



ABSTRACT : PROBLEM TO BE SOLVED: To perform filling by the film of a low dielectric constant, high reliability and high productivity so as to reduce the capacity of a groove part between the wirings of a wiring pattern in an inter-layer insulation film for the multi-layer wiring of VLSI and to accelerate the operation speed of a semiconductor device.

SOLUTION: An inter-layer insulation film is turned to the three-layer structure of a fine and high quality silicon oxide film (SiO_2) 41, a porous silicon oxide film (SiO_x ; $x < 2$) 42 and the fine and high quality silicon oxide film (SiO_2) 43. Continuous film formation is made possible just by changing the process conditions of a high density plasma CVD method, planarization is performed by applying CMP (ultraprecise chemical and mechanical polishing).

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